Chris Repanich

CECS 341

Lab 1: 2 to 1 Mux 32bit

**Verilog Source Code:**

//////////////////////////////////////////////////////////////////////////////////

// Christopher Repanich

// Lab1: Mux2to1\_32bit

// Description: 2 to 1 32 bit multiplexer

//////////////////////////////////////////////////////////////////////////////////

module Mux2to1\_32bit(Sel, DataIn0, DataIn1, DataOut);

input Sel;

input [31:0] DataIn0, DataIn1;

output reg [31:0] DataOut;

always@(Sel, DataIn0, DataIn1)

begin

case(Sel)

1'b0: DataOut <= DataIn0;

1'b1: DataOut <= DataIn1;

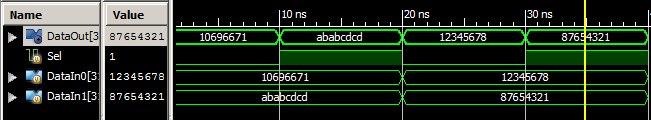
default: DataOut <= 32'bX; //assign X unknown by defaults

endcase

end

endmodule

**Simulation Results:**



**Test Fixture: (Asked to include this on the dropbox page)**

module Mux2to1\_Tester;

// Inputs

reg Sel;

reg [31:0] DataIn0;

reg [31:0] DataIn1;

// Outputs

wire [31:0] DataOut;

// Instantiate the Unit Under Test (UUT)

Mux2to1\_32bit uut (

.Sel(Sel),

.DataIn0(DataIn0),

.DataIn1(DataIn1),

.DataOut(DataOut)

);

initial begin

// Initialize Inputs (first test case)

Sel = 0;

DataIn0 = 32'h10696671; //random value (student ID missing first digit)

DataIn1 = 32'hABABCDCD; //random value

#10; //10 unit time delay

//Test Case 2

Sel = 1;

#10;

//Test Case 3

Sel = 0;

DataIn0 = 32'h12345678; //random value (student ID missing first digit)

DataIn1 = 32'h87654321; //random value

#10;

Sel = 1;

#10;

$stop;

end

endmodule